CI13162P Data Sheet

High cost performance neural network intelligent voice chip

- **Brain Neural Network Processor (BNPU)**

--BNPU V3.5, supports DNN\TDNN\RNN\CNN and other neural networks and parallel vector operations, can achieve high performance speech recognition and call noise reduction and other functions

CPU and memory

--CPU frequency up to 210 MHz

--Built-in 2MBytes Flash memory

-Built-in 288KBytes SRAM

- Built-in 256-bit eFuse for application encryption

- **Audio Codec**

-High performance low power consumption audio ADC, SNR ≥ 95dB

-Low power consumption audio DAC, SNR ≥ 95dB

- **PWM**

-Supports 3 PWM interfaces

- **GPIO**

--4 high-speed GPIO with a flip frequency up to 20MHz

-4 GPIO channels support 5V level communication

- **Reset and power management**

-Supply voltage range 3.6V～5.5V

-Built-in PMU power management unit

-Built-in power-on reset (POR)

-Built-in voltage detection (PVD)

- **clock**

-Built-in RC oscillator

-Support for external crystal oscillator input

- **communication interface**

-1 IIC interface

-2 UART interfaces, support 5V level communication, up to 3Mbps communication rate

- **Timer and watchdog**

-Built-in 2 sets of 32-bit timers and 1 watchdog

- **power amplifier**

-Maximum drive power is 2.0W (4Ω load)

--No output coupling capacitor or external buffer circuit is required

catalogue

1 Summary

1.1 Functional description

The CI13162P is a next-generation high-performance neural network smart voice chip developed by Chipintelli. It integrates the company's proprietary Brain Neural Network Processor (BNPU) V3.5 and CPU core, delivering a system clock rate of 210MHz. Featuring 288KB of built-in SRAM, the chip incorporates a Power Management Unit (PMU) and RC oscillator, along with a 2W audio amplifier that eliminates the need for external amplifiers. The design includes a single-channel high-performance low-power Audio Codec and multiple peripheral control interfaces such as UART, IIC, PWM, and GPIO. With minimal external components like resistors and capacitors, the CI13162P enables hardware solutions for various smart voice products while maintaining exceptional cost-effectiveness.

CI13162P adopts industrial design standards, has good environmental reliability, its working temperature range-40℃ ~ +85℃, in line with MSL3 grade of moisture sensitivity, in line with IEC 61000-4-2 of 4KV contact discharge test standard, in line with RoHS and REACH environmental protection standards.

The CI13162P leverages Chipintelli's next-generation BNPU technology, which supports neural networks (DNN/TDNN/RNN/CNN) and parallel vector operations. This enables high-performance speech recognition, noise reduction, and exceptional environmental noise suppression capabilities. The solution supports multiple global languages including Chinese, English, and Japanese, making it widely applicable across industries such as home appliances, lighting, toys, wearables, industrial equipment, and automotive sectors. It facilitates voice interaction control and various intelligent voice application scenarios.

1.2 Chip specifications

The function block diagram of CI13162P is shown in Figure 1-1:

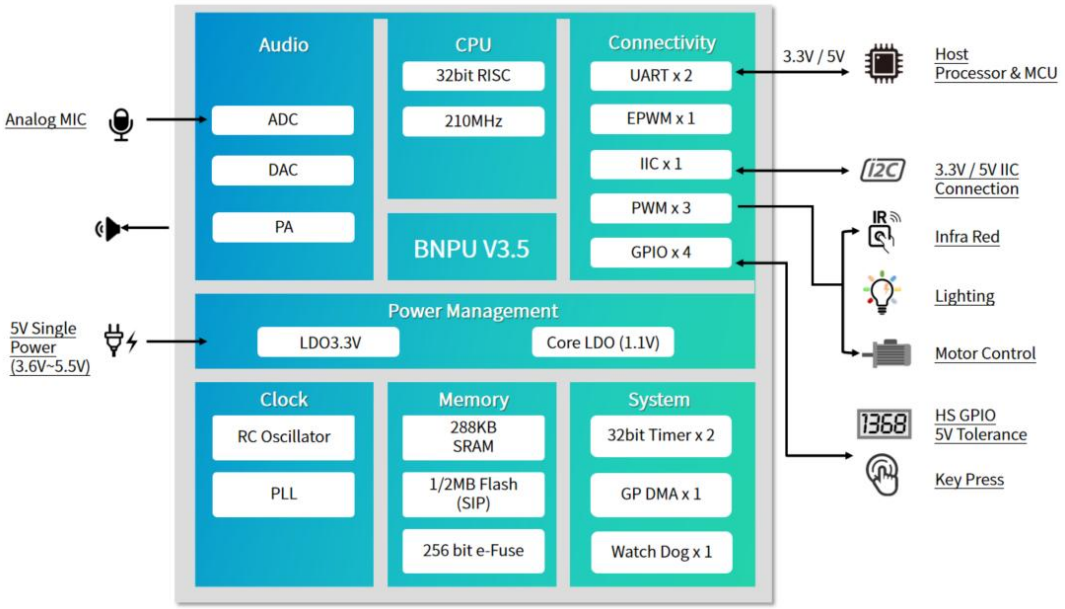


Figure 1-1 CI13162P function block diagram

- **Brain network processor BNPU V3.5**

-It adopts the new generation of Chipintelli hardware BNPU technology, supports DNN\TDNN\RNN\CNN and other neural networks and parallel vector operations, and can realize high performance speech recognition, speech noise reduction and other functions

- **CPU**

-32-bit high performance CPU, up to 210MHz operating frequency

- **Memory**

-Built-in 288KB SRAM

-Built-in 256bit eFuse

-Built-in 2MB Flash

- **Audio interface**

-Built-in high performance low power Audio Codec module, support single channel ADC sampling and single channel DAC playback

-Support for Automatic Level Control (ALC)

-Support for 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz sampling rate

- **Power management unit PMU**

-Support wide power supply voltage, power supply range 3.6V～5.5V

-Built-in 2 high performance LDO circuits, no need to configure external power chip, application scheme only needs a small number of peripheral components

- **Clock**

  -Built-in RC oscillator

  -Support for external crystal oscillator input

- **External devices and timers**

  -2 UART interfaces, support up to 3M baud rate communication

  -1 IIC interface, which can be connected to IIC devices for expansion

  -3 PWM interfaces, which can be directly driven for lamp control and motor applications

  -Built-in 2 sets of 32bit timers

  -Built-in 1 independent watchdog (IWDG)

- **GPIO**

  -Supports 4 GPIO ports and can be used as main control IC

  -Each GPIO port can be configured with interrupt function and pull-up/down state

  -4 GPIO channels can directly support 5V level communication through an external 5V pull-up resistor

- **Power amplifier**

  -Maximum drive power is 2.0W (4Ω load)

  --No output coupling capacitor or external buffer circuit is required

  --Stable gain output

  --External gain Settings

  --Noise suppression for power on and power off

- **Software development support**

  -Provide complete software development kits, application solution examples, direct online firmware development using the voice development platform and other support. For details, please visit: https://aiplatform.chipintelli.com

- **Firmware burning and protection**

  -Support UART upgrade and firmware protection

- **ESD function**

  -Internal ESD enhanced design, which can pass 4KV contact discharge test

- **ROHS and REACH**

  -Use of environmentally friendly materials, support RoHS and REACH standards

- **Encapsulation and operating temperature range**

  -Packaging form: SOP16, size of 9.9mm long, 6.0mm wide and 1.7mm high

  -Working environment temperature: -40℃ ~+85℃

2 Pin diagram and function description

2.1 Pin diagram

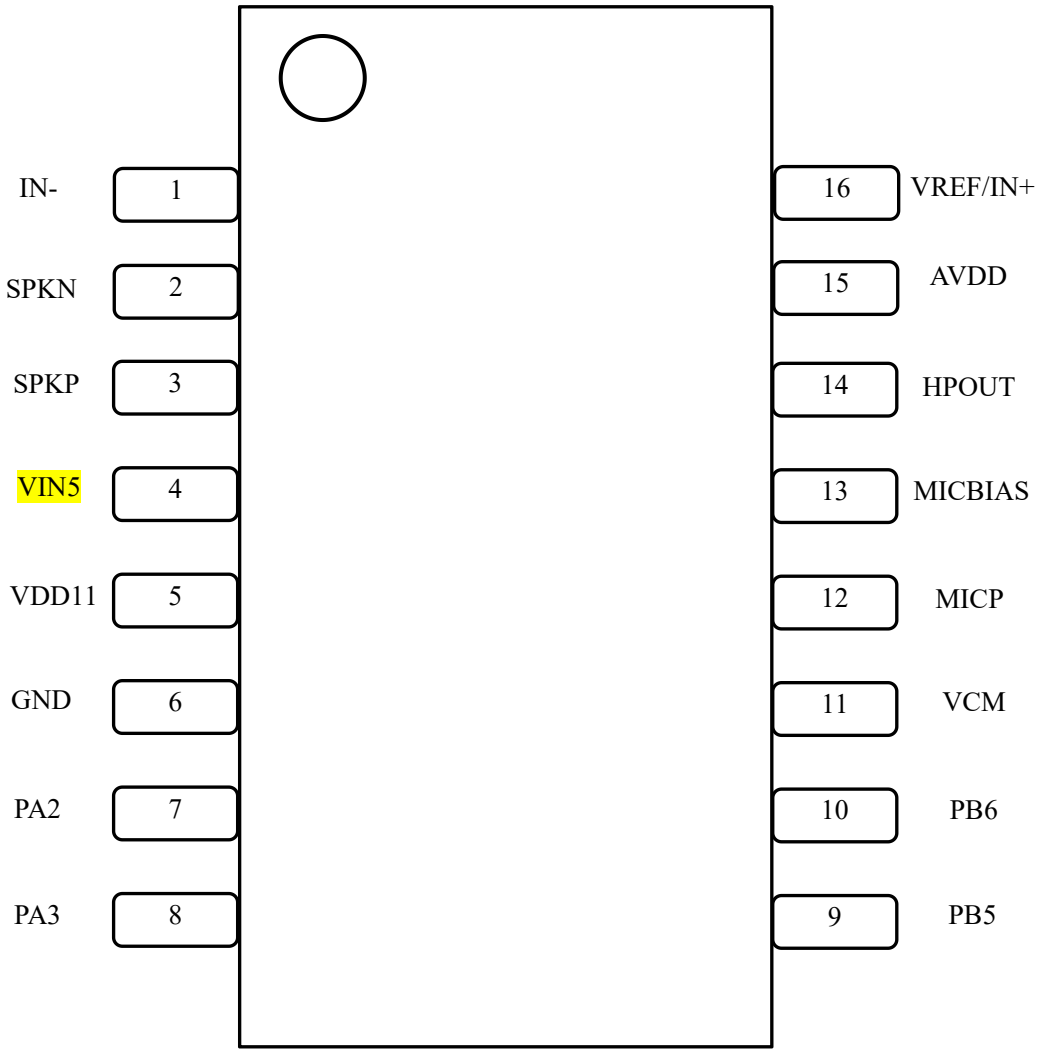


Figure 2-1 CI13162P pin sequence and definition Figure

2.2 Pin Description

Pin description Table 2-1

Pin Number	Pin Name	Type	5V Tolerant	Power-on Default State	Pin Function
1	IN-	IO	-	-	● Power amplifier reverse input
2	SPKN	IO	-	-	● Power amplifier N-end output
3	SPKP	IO	-	-	● Power amplifier P terminal output
4	VIN5V	P	-	-	● Power supply voltage input, power supply voltage range 3.6V～5.5V * Note1*
5	VDD11	P	-	-	● LDO-1.1V output ● The kernel has a 1.1V power supply input * Note1*
6	GND	P	-	-	Ground
7	PA2	IO	√	IN，T+D	● GPIO PA2 (default state on power up) ● IIC_SDA ● UART1_TX ● PWM0 ● PWMP
8	PA3	IO	√	IN，T+D	● GPIO PA3 (default on power up) ● IIC_SCL ● UART1_RX1 ● PWM1 ● PWMN
9	PB5	IO	√	IN，T+U	● GPIO PB5 (default on power up) ● UART0_TX ● IIC_SDA ● PWM1 ● PWMP
10	PB6	IO	√	IN，T+U	● GPIO PB6 (default on power up) ● UART0_RX ● IIC_SCL ● PWM2 ● PWMN
11	VCM	O	-	-	● VCM POWER Output ● PGEN * Note2 *
12	MICP	I	-	-	Microphone P input
13	MICBIAS	O	-	-	Microphone bias output
14	HPOUT	O	-	-	DAC output
15	AVDD	P	-	-	● Internal LDO-3.3V output ● Internal analog circuit 3.3V power supply input * Note1*
16	VREF/IN+	IO	-	-	● Power amplifier voltage reference terminal

Note1 The pin needs to be connected to a 4.7uF capacitor

Note2 This pin is high when powered on, and the system will enter programming mode

The 11VCM (PG_EN) pin is configured with default internal pull-down. When the system detects a high-level signal on this pin during power-on and receives a firmware upgrade command from the UART0 interface, it automatically enters upgrade mode, allowing programming of the chip's internal Flash memory through the upgrade tool. If no firmware upgrade command is detected on the UART0 interface or the VCM pin voltage remains low, the system will revert to normal operation mode.

symbol definition ：

I import I import

O output O output

IO two-way IO two-way

P Power or ground P Power or ground

T+D three-state down T+D three-state down

T+U Tri-State Pull-Up T+U Tri-State Pull-Up

OUT The default output of the power supply OUT The default output of the power supply

IN Upper power default input IN Upper default input

All IOs can be configured with drive capability and pull-up/down status.

2.3 IO Multiplexing Functionality

Table 2-2 IO multiplexing functions

Pin Name	Function1	Function2	Function3	Function4	Function5	Function6
PA2	PA2	-	IIC_SDA	UART1_TX	PWM0	PWMP
PA3	PA3	-	IIC_SCL	UART1_RX	PWM1	PWMN
PB5	PB5	UART0_TX	IIC_SDA	PWM1	PWMP	
PB6	PB6	UART0_RX	IIC_SCL	PWM2	PWMN	

3 Electrical character

Table 3-1 Electrical characteristics table

Symbol	Description	Min	Type	Max	Unit
VIN5V	Chip power input *Note1*	3.6	5.0	5.5	V
AVDD	3.3V power supply	2.97	3.3	3.63	V
VDD11	1.1V power supply	0.99	1.1	1.21	V
VIH	Enter a high level （3.0V ≤VDD33 ≤ 3.6V）	0.7× VDD33	-	VDD33+0.3	V
VIL	Input low level （3.0V ≤ VDD33 ≤ 3.6V）	-0.3	-	0.3× VDD33	V
VOL	Output low level @IOL = 12mA	-	-	0.4	V
VOH	Output high level @IOH = 20mA	2.4	-	-	V
I5V-IO	Drive current at 3.3V when the 5V voltage IO port is output	20	-	33	mA
I3V3-IO	3.3V voltage withstand IO output 3.3V drive current	14	-	24	mA
ΣIVDD	The sum of all the total currents of the chip	-	-	200	mA
Pde	The chip uses 5V power supply and VDD11 uses external supply 1.1V state. The total power consumption of 5V power supply (TA = 25 ° C) is normal when recognized	60	-	110	mW
Pdi	The chip is powered by 5V and the system is powered by internal LDO. The total power consumption of the 5V input (TA = 25 ° C) is normally recognized	145	-	275	mW
Pa	The chip is powered by 5V and the system is powered by internal LDO. The total power consumption of the 5V input (TA = 25 ° C) during normal broadcast	1.375	-	2.675	W
Precision of RC oscillator *Note2*	TA：-40℃～+85℃	-1.5	-	+1.5	%
Top	Chip operating temperature	-40	-	+85	℃
Tst	Chip storage ambient temperature	-55	-	+150	℃

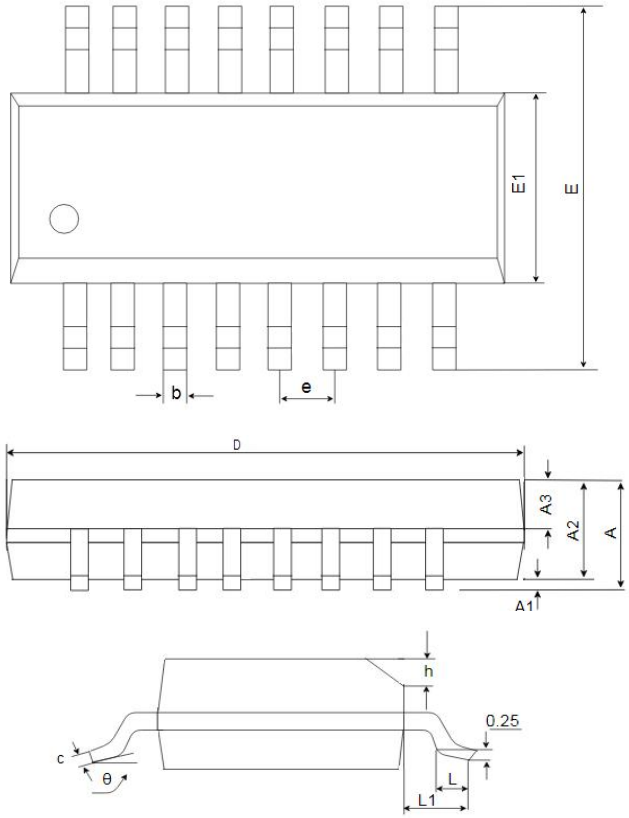
Note1: The ripple is required to be less than 300mVp-p.

Note 2: Due to semiconductor technology principles and characteristics, the built-in RC oscillator in chips may exhibit temperature drift (±1.5%) in extreme environments. The CI13162P chip incorporates a baud rate adaptive circuit to ensure stable communication with host computers across varying temperatures. For applications requiring ultra-precise clock synchronization, please use our externally crystal-configured chips and corresponding implementation solutions.

Power amplifier parameters

parameter	symbol	test condition	MIN	TYP	MAX	unit
Output power 8Ω	Po	THD+N<1%，f=1KHZ		1.1		W
		THD+N<10%，f=1KHZ			1.6	W
Output power 4Ω		THD+N<1%，f=1KHZ		1.6		W
		THD+N<10%，f=1KHZ			2.4	W
Total harmonic + distortion noise	THD+N	PO=0.5Wrms；f=1KHZ		0.1	0.2	%
supply voltage rejection ratio	PSRR	Vripple=200mVPP, sine wave Wave, input connected to 10Ω resistor	60	63@f=217Hz 68@f=1KHz		dB

4 Packaging information



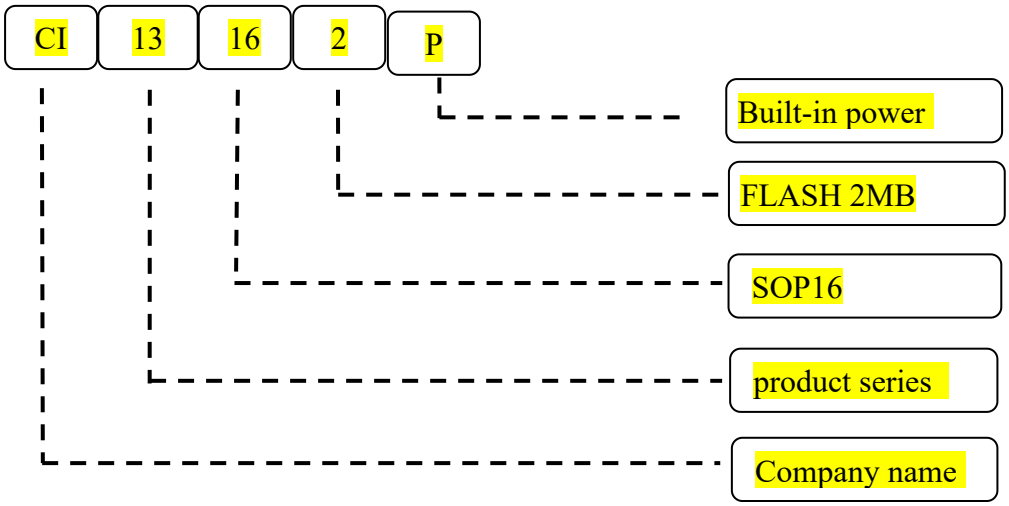
COMMON DIMENSIONS

SYMBOL	UNIT：MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.70
A1	0.10	_	0.225
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
b	0.39	_	0.47
c	0.20	_	0.24
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	_	0.50
L	0.50	0.6	0.80
L1	1.05REF		
θ	0	_	8°

5 Order information

The chip package MRAK of CI13162P is shown in the figure below. The first line is the company LOG, the second line is the chip model, the third line is the production batch number, and the dot in the lower left corner is the identification of pin 1.

The chip model is defined as follows:



The order information of CI13162P chip is shown in Table 5-1.

Table 5-1 CI13162P chip order information table

product model	Encapsulation form	Basic packaging	Number of tubes installed	Factory standard package	Standard package quantity
CI13162P	SOP16	Tube	50pcs	box-packed	10000pcs (200 tubes/box)

6 Application

6.1 Application reference circuit diagram

The CI13162P chip requires only a small number of peripheral components to develop terminal product solutions that support various voice applications. The CI13162P supports a single microphone and single end input, a single speaker broadcast output, and a maximum speaker support of 4 ohms and 2.4W.

The following is an example of the typical application scheme of CI13162P to introduce the key points and precautions of application scheme design

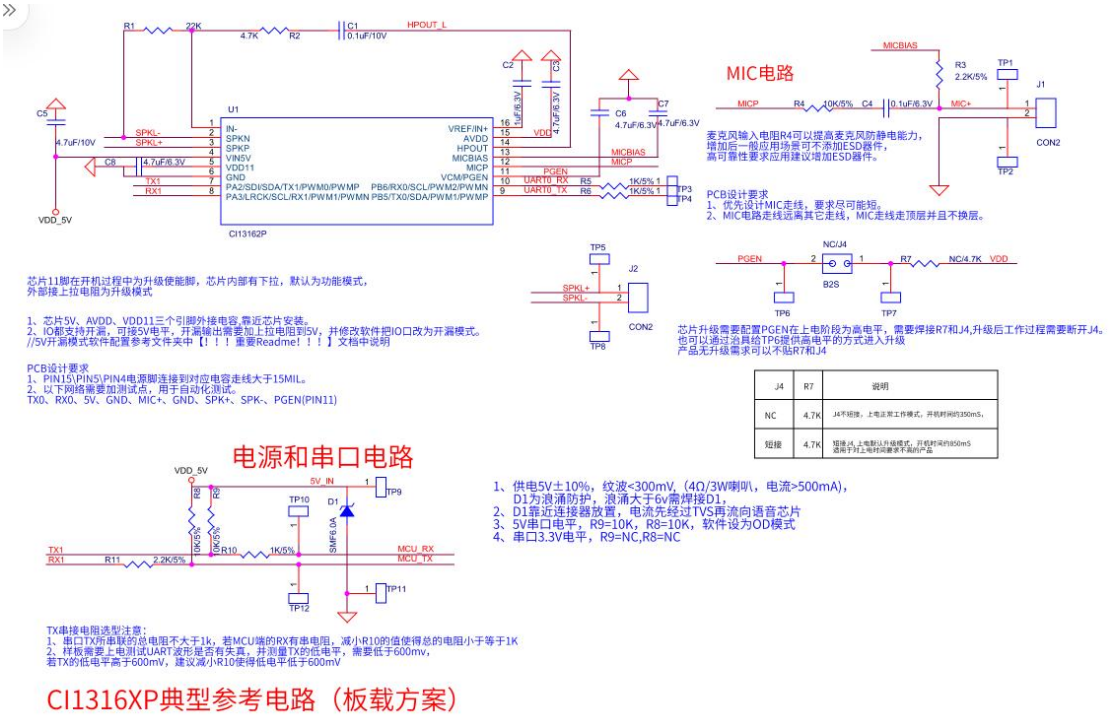


Figure 6-1 Typical application scheme reference circuit diagram of CI1316XP

The diagram above shows a reference circuit design for typical applications of the CI1316X series chips (including CI13162P) with single-microphone input and power amplifier output. This design is not limited to specific end products. The application solution should be developed based on compatibility with host computer terminal products, and reference schematics and PCB layouts can be downloaded from the Chipintelli Documentation Center and AI Platform according to the functional and performance requirements of the terminal device. Documentation Center linkhttps://document.chipintelli.com/

If the board-level upgrade function needs to be reserved during the application scheme design, UART0 pins can be led out as sockets or test points, so as to facilitate the firmware burning or upgrading through UART0 after the PCB board is soldered.

The VCM/PGEN pin on CI13162P chip is preconfigured with a pull-down resistor. During power-on, the system checks if this pin is pulled to 3.3V high level by an external pull-up resistor.

If the UART0 pin receives an upgrade signal from external input at this elevated state, the system enters upgrade mode. If no external pull-up resistor is connected to this pin, the chip skips the upgrade mode detection and directly enters normal boot mode, enabling rapid system startup. For applications requiring fast boot, the VCM/PGEN pin can be routed externally with a jumper wire connected to a 4.7KΩ resistor pulling up to VDD33. This configuration enables normal boot mode during power-on, reducing boot time to approximately 350ms. To enable online upgrades, short-circuit the jumper wire or its test points to pull the PGEN pin to 3.3V high level via UART0 port. If no fast boot is required, disconnect J4 jumper wire. Refer to the original application diagram for detailed implementation or consult our FAE. The two operating modes of PGEN are listed in the table below:

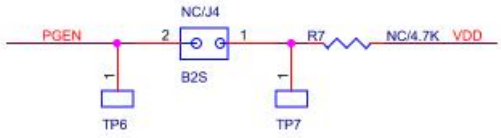
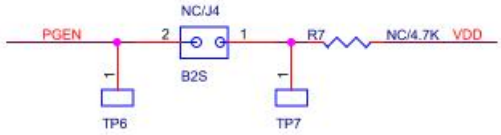
PG_EN working mode diagram	Installation status of J4	PG_EN high and low levels	available machine time
	short circuit	High level, upgrade mode	850ms
	open a way	Low level, working mode	350ms

Table 6-1 CI1316X Upgrade Mode Table

CI13162P supports single-ended microphone input, which is only recommended for the scheme where the microphone input line length is less than 20 cm. Otherwise, the microphone input line is too long, which will affect its anti-interference ability and lead to poor speech recognition effect.

If the application scheme does not require ultra-low power consumption, it is recommended that the design scheme use the PMU in CI13162P to reduce the cost. If the application scheme requires ultra-low power consumption, an external DCDC circuit can be used to supply 1.1V to CI13162P to reduce the system power consumption.

The UART ports of CI13162P can support 5V level communication. The UART0 port in the figure above uses 3.3V communication level as an example. If the application scheme needs to connect to 5V communication level, a 5V pull-up resistor can be added around the RX and TX pins of UART0 without configuring a level conversion circuit.

6.2 Other application notes

1. CI13162P is manufactured with lead-free and environmentally friendly materials. When SMT welding, please set the furnace temperature and time parameters according to lead-free standards as shown in the figure below

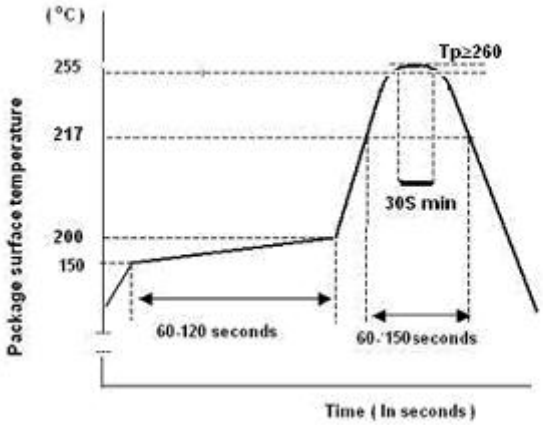


Figure 6-2 Furnace temperature curve

2. Attention should be paid to anti-static measures during the use, handling and production of CI13162P, and its packaging should be made of anti-static materials.

- Chipintelli reserves the right to interpret and change this specification. If there is any change, we will not give further notice! Customers should obtain the latest version of the data before application design, and verify whether the relevant information is accurate and complete.
- Any semiconductor product may fail or malfunction under certain conditions. The chip application party is responsible for complying with safety standards and taking safety protection measures when using the product for system design and complete machine manufacturing, so as to avoid personal injury or property loss caused by possible product failure!
- Chipintelli will do its best to provide customers with better products and better services!